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QUARTERLY REPORT NO. 9
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314

1 April 1989—30 June 1989

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13500 N. Central Expressway
P.O. Box 655936, M.S. 105
Dallas, Texas 75265
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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a high-sampling-rate GaAs A/D converter and a high-resolution GaAs A/D converter.

B. ADC Status

The world's first reported GaAs 5-bit analog-to-digital converters have been fabricated by Texas Instruments with 16% yield. Two 5-bit ADC chips from one wafer were packaged in a specially designed hybrid package and tested by Hughes at clock frequencies up to 400 MHz. These devices, which are building blocks for the radiation-hard monolithic 12-bit ADC to be fabricated for SDIO, exhibited excellent signal-to-noise ratios and linearities.

Key analog building blocks of the 12-bit ADC, which include a sample-and-hold, gain-switched amplifier, 8-bit digital-to-analog converter (DAC), and 5-bit ADC have been designed, the photomask received, and three lots started. Information gained from wafer testing the building blocks in August will be folded into the complete SDIO 12-bit ADC scheduled to start fabrication in September 1989.

System-level design and the majority of circuit design for the complete monolithic 12-bit ADC are complete. Layout capture of the rad-hard 12-bit ADC will be completed by the end of next quarter, with mask release scheduled for the end of September. Finally, a rough-order-of-magnitude cost estimate for adding a 16:1 analog multiplexer and front-end prescaler to the 12-bit ADC have been completed by Hughes and a white paper is being prepared for the DARPA program office.

A new contact metal system using palladium/germanium (Pd/Ge) in lieu of AuGe/Ni has demonstrated reduced contact resistivity on pilot lots. These improvements, when demonstrated on actual lots, should result in improved ADC performance. High-energy (4.5 MeV) oxygen implants are being evaluated as a means to isolate individual transistors. Initial results from ADC lots show somewhat better isolation characteristics when compared to our standard trench-isolation process. The oxygen-implant process permits increased circuit density for reduced chip cost and improved circuit performance.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. ADC Process Status

Photomasks for the new 5-bit ADC design, in which the $7 \times 7 \mu\text{m}^2$ emitter transistors in the original design have been replaced by $5 \times 5 \mu\text{m}^2$ emitter transistors, have been received and three lots have been started. This mask set contains several building blocks for the 12-bit ADC that were not included in the original design. These building blocks include a new sample-and-hold circuit, an 8-bit digital-to-analog converter, and a gain-switched amplifier. Texas Instruments will attempt to complete processing on these lots in time for Hughes to characterize the circuits prior to releasing the 12-bit ADC mask set in September. This will allow minor design tweaks prior to releasing the 12-bit design based on the electrical results from the new 5-bit ADC lots if required.

B. HBT Contact Resistance Development

While we have made significant improvements in the ohmic contact process during the past few months, contact resistance (R_c) for $7 \times 7 \mu\text{m}^2$ emitter HBTs still varies between 16 and 60 ohms, depending on the particular lot. The ADC lot with 16% yield for the 5-bit ADCs averaged 16 ohms for emitter resistance, corresponding to a specific contact resistivity of $4 \times 10^{-6} \text{ ohm-cm}^2$. On a recent lot delivered to Hughes (Lot 106112), emitter resistance varied between 30 and 60 ohms. While this lot yielded several partially functional ADCs, the high emitter resistance was credited for the lack of fully functional chips. The difference between the fully functional lot and the latest lot was approximately a worst-case increase in emitter resistance of only a factor of four. This suggests the AuGe/Ni process is still marginal and that a process with a larger manufacturing tolerance is required.

Even with the low value of $2 \times 10^{-6} \text{ ohm-cm}^2$ for our standard AuGeNi process the emitter resistance on the $5 \times 5 \mu\text{m}^2$ devices would be 22 ohms, which is marginally too high. One way to make a low contact resistivity n-ohmic would be to make the GaAs cap layer thicker and highly doped; however, this would conflict with the integration of the n-JFET with the HBT. Our experiments with thicker cap layers indicate it is difficult to remove the cap layer selectively in those areas where it would allow a leakage path without adversely affecting the bipolar transistor. The alternative to continued work on small variations in the AuGeNi process or the thicker epi is to examine a different metal system.

Any new contact system will have to satisfy at least two requirements: (1) contact resistivity must be less than our best AuGe/Ni, and (2) contact metallurgy must not spike through the GaAs emitter contact and short the base-emitter junctions. The Pd/Ge contact system, which has been shown in the literature to yield low contact resistivity and no spiking from the solid phase reaction

it undergoes with GaAs, represents a potential replacement for our standard AuGe/Ni system. Toward that end TI is evaluating the PdGe contact system with IR&D funding. This work is being reported here since improvements in the contact resistivity will impact ADC performance, as well as TI internal GaAs HBT programs.

S.S. Lau and L.C. Wang at University of California at San Diego have been helpful through many conversations in demonstrating the PdGe metal process to us and in helping to implement the PdGe evaporation and anneal procedure here at TI. The contact resistance of PdGe was examined by preparing a series of pilots with Si implanted into transmission-line channels in semi-insulating GaAs and using RTA to activate the Si. These pilots were then used for transmission-line measurements using an auto-probe measurement system. The doping density of the Si after activation at 950°C corresponds to $\sim 1.5 \times 10^{18}/\text{cm}^3$. Several different experiments between TI and S.S. Lau's group demonstrated very promising results. When the metallurgy and anneal were all done at UC the Pd contact resistivity, R_c , was $8.9 \times 10^{-7} \pm 1.7 \times 10^{-7} \text{ ohm-cm}^2$; while a control wafer processed at TI using AuGeNi gave R_c of $2.2 \times 10^{-6} \pm 1.3 \times 10^{-6} \text{ ohm-cm}^2$. On a full wafer with the metallurgy done at UC and the anneal done at TI, seventy-five transmission-line measurements were made giving a median contact resistivity of $1.03 \times 10^{-6} \pm 1.4 \times 10^{-7} \text{ ohm-cm}^2$.

We then implemented the entire process in our lab and set about evaluating the temperature stability of the PdGe contact. A series of wafers was prepared with Si implantation and annealing at 850°C or 950°C, which results in doping densities of 6×10^{17} or $2 \times 10^{18}/\text{cm}^3$, respectively. The PdGe process used was as close to the UC description as we could make it. After annealing the PdGe alloy at 325°C for 30 min the wafers were broken into quarters so that additional anneals of 10 sec duration could be done at 350°C, 400°C, and 450°C, leaving one quarter as processed. The results were good. Figure 1 shows transmission-line contact resistivity as a function of anneal temperature. The as-processed n-ohmics (325°C) are $7.3 \times 10^{-7} \text{ ohm-cm}^2$, which is an excellent value. This would result in an emitter resistance of 3 Ω for a $7 \times 7 \text{ } \mu\text{m}^2$ emitter device and 8 Ω for a $5 \times 5 \text{ } \mu\text{m}^2$ device. Postprocessing temperatures of 400°C or greater do degrade the contact by an amount that increases with increasing temperature. Uniformity remains good even during the degradation. The higher doping density of the 950°C Si anneal substrates clearly gives better contact resistivity.

Kelvin contact structures were also examined. The effect of the postprocessing anneals on contact resistivity for square Kelvin contacts with sides of 5, 7, 20, or 30 μm is shown in Figure 2. Anneals degrade the contacts, regardless of contact size. The ideal ohmic contact would give the same contact resistivity regardless of size. These PdGe contacts display some tendency to be better in large-area contacts. This can be seen in Figure 2 and is plotted specifically in Figure 3. However, the data in Figure 3 form almost a straight line within the error bars, indicating minimal size effect. More will have to be done to assure that the PdGe can scale to micrometer sizes. Further samples

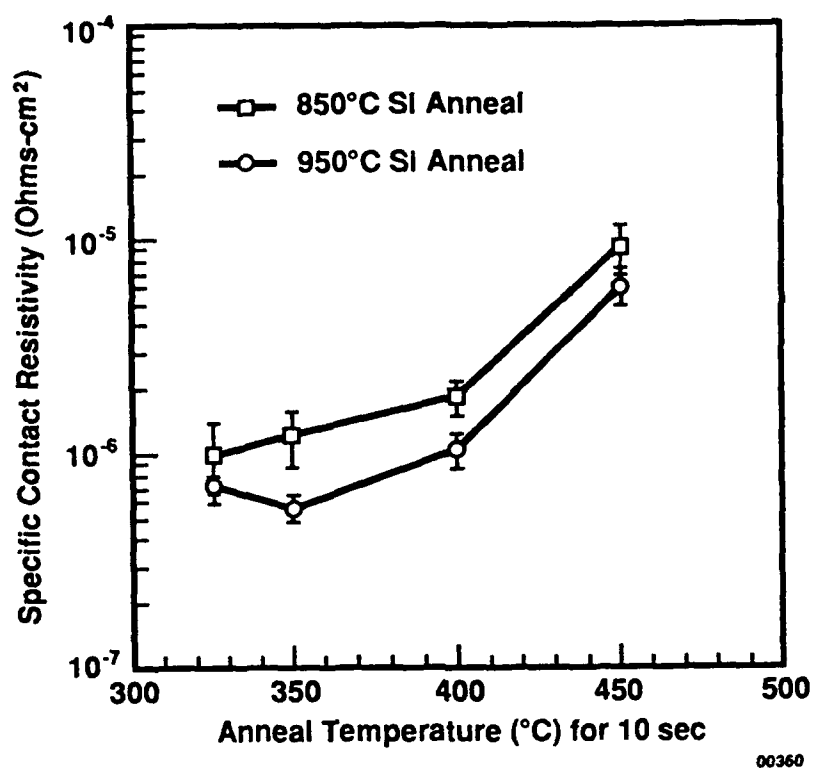


Figure 1. Transmission-line contact resistivity as a function of anneal temperature.

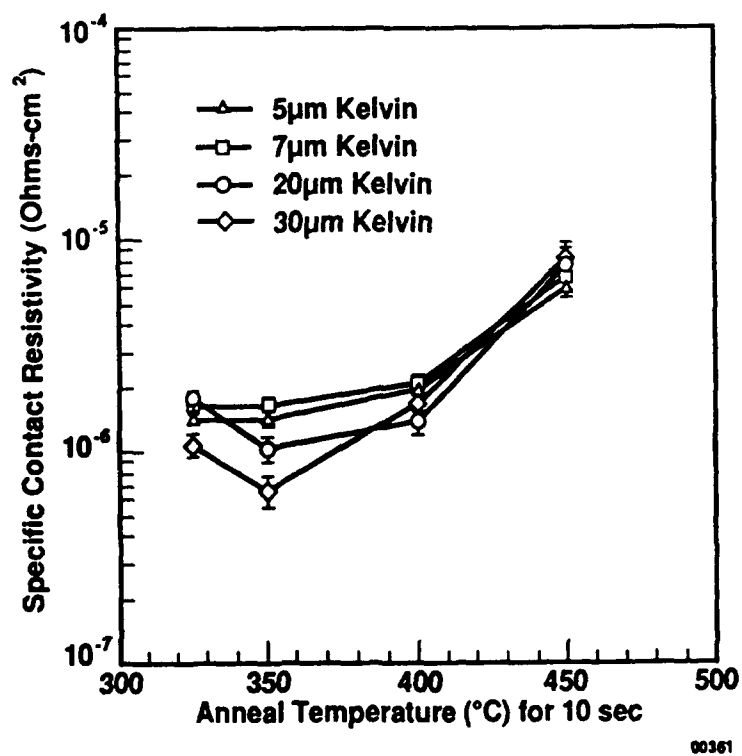
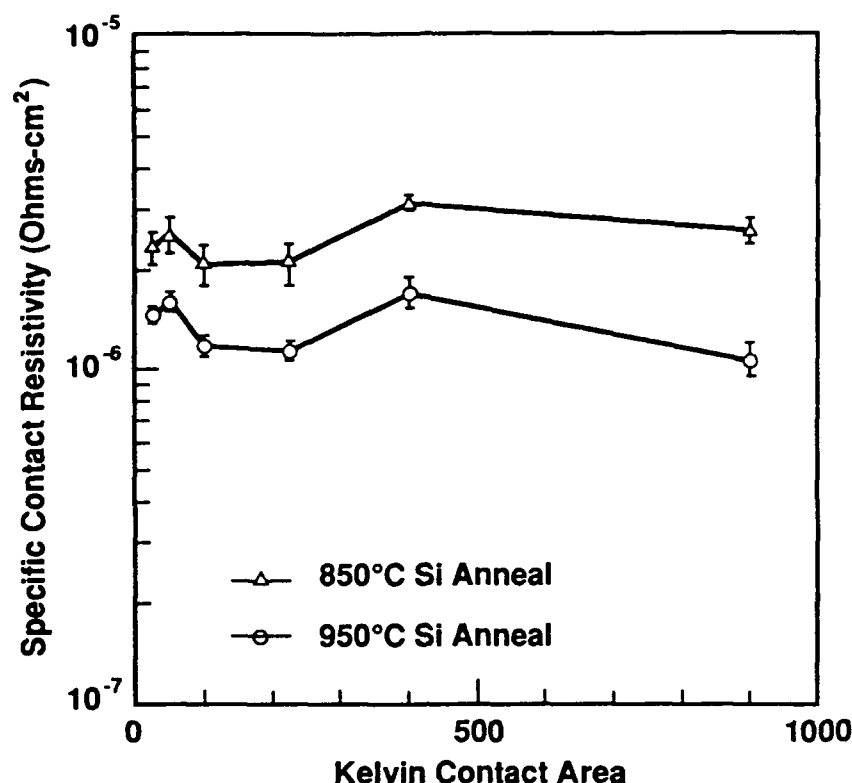


Figure 2. PdGe n-ohmic degradation with increasing temperature.



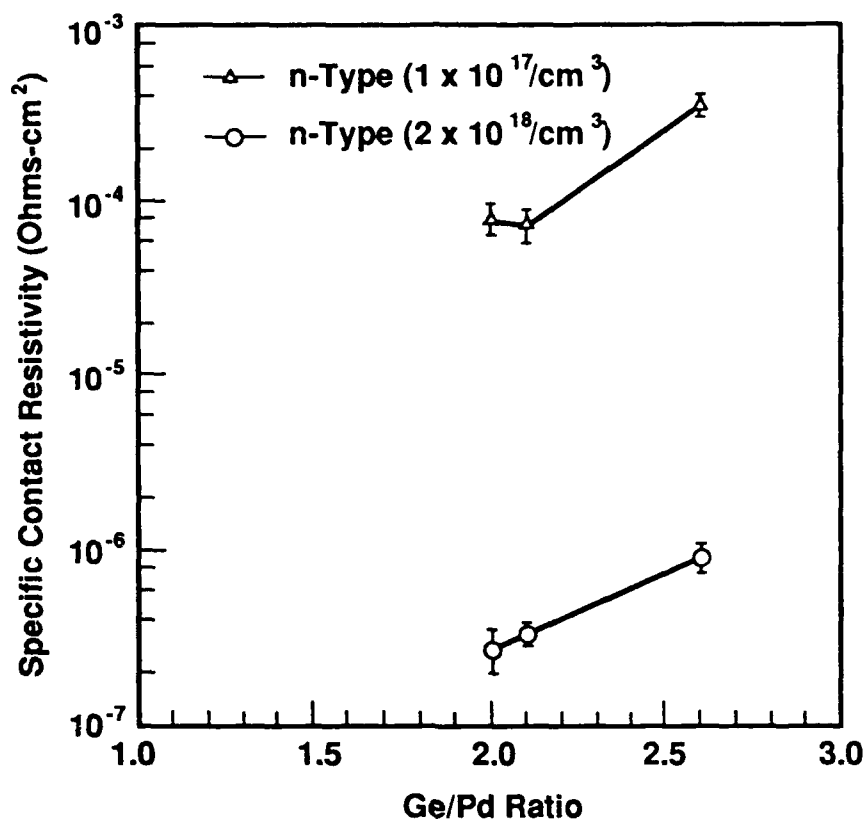
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Figure 3. PdGe n-ohmic behavior with Kelvin contact area.

where the metallurgy was done at UC and the probing at TI indicate that the optimum Ge to Pd ratio has not yet been achieved. The metallurgy used at TI to date has resulted in a Ge to Pd ratio of 2.6. Figure 4 illustrates that as the Ge to Pd ratio is decreased, contact resistivity decreases. This reduction occurs for both highly doped material ($\sim 2 \times 10^{18}/\text{cm}^3$) and lighter doped material ($\sim 1 \times 10^{17}/\text{cm}^3$). However it is still evident that highly doped material is necessary to get low contact resistivity.

Test lots are being run to examine these several integration issues in addition to tests on optimizing the Ge to Pd ratio. We will probably venture one or two wafers out of a real lot to evaluate the PdGe process on real material and assume we can make a good overlayer. If successful, this would have tremendous payback. The following aspects of the PdGe process remain to be analyzed.

- Can the Pd/Ge contact be alloyed with an Au or TiN/Au overlayer, which is necessary as an etch stop for our via process? Our present via etch process will etch Ge, potentially degrading the contact.
- Will Pd/Ge make good contact to our emitter layer on a real device?
- Will PdGe and the necessary overlayer degrade during repeated heating and cooling of the trench isolation and double-level metal interconnect process?



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Figure 4. Effect of n-ohmic Ge to Pd ratio.

- Are there negative consequences to moving the AuZn process position to one in front of the PdGe contact, (AuZn contact needs 370°C, which would degrade the PdGe).

These are issues that we need to address before we can declare the PdGe process a success. However, Pd/Ge contact resistivity looks promising.

C. Advanced HBT Isolation Process Development

Implant damage is being investigated as an alternative to the use of a trench to isolate the individual transistors on the ADC chip. This will allow for improved packing densities and reduced capacitances compared to our trench process. Oxygen is implanted at 4.5 MeV, resulting in a damage region extending completely through the n⁺ buried collector region. This eliminates the n⁺ region from field and resistor areas and therefore significantly lowers circuit capacitance. The first ADC lot using oxygen implant as an isolation procedure has been completed. The first question to be answered was whether the transistors were isolated from each other. Figure 5 illustrates the transistor-to-transistor leakage current as a function of bias for temperatures ranging from 50 °C to 250 °C. Leakage current at 10 V is plotted versus 1/temperature in Figure 6, along with a similar plot

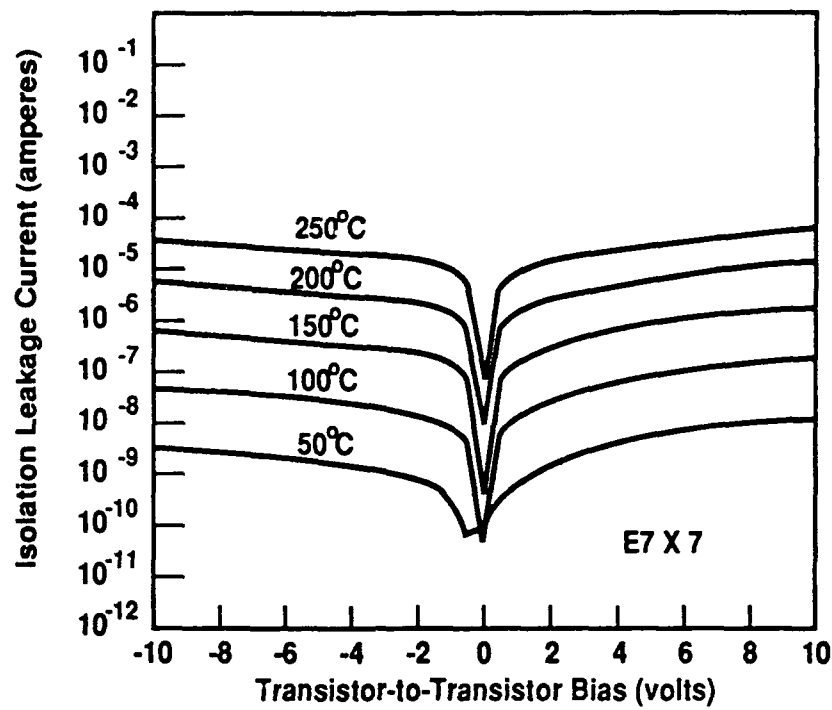


Figure 5. Transistor-to-transistor leakage current.

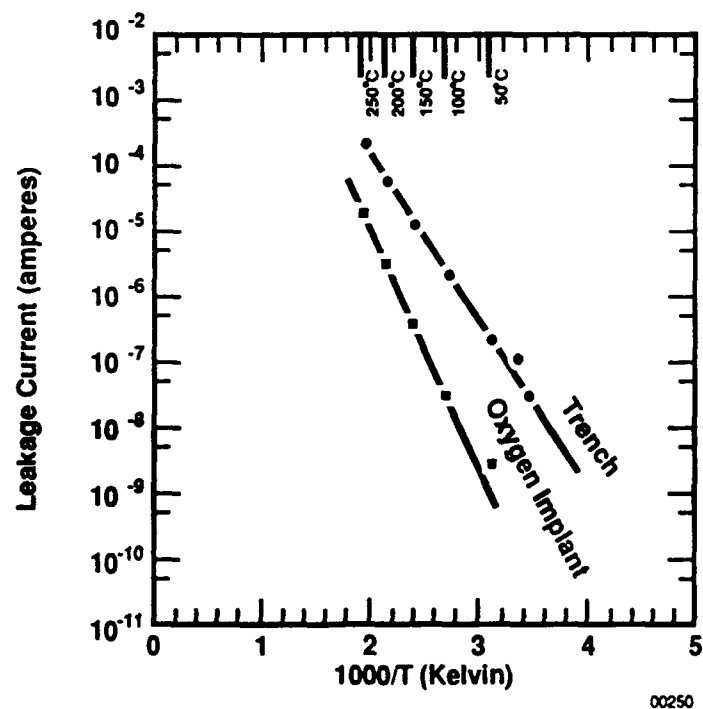


Figure 6. HBT isolation leakage current.

degrade dc performance of ADC circuits. A more complete evaluation of this isolation process will be done prior to making any changes in the base process.

III. CIRCUIT DESIGN/TESTING

Toward the program goal of fabricating a complete 12-bit 20 Msps/W ADC, a mask set containing all the key analog building blocks including a 12-bit sample-and-hold (S/H), gain-switched amplifier, 8-bit digital-to-analog converter (DAC), and 5-bit quantizer was released for processing at the beginning of the quarter. Information gained from wafer testing of the 12-bit building blocks will be folded into the complete monolithic 12-bit ADC design schedule for mask release in September.

The Hughes portion of the $5 \times 5 \mu\text{m}^2$ 12-bit building block mask set, released in April 1989, is pictured in Figure 7. The mask set contains S/H input buffer and hold amplifiers, sampling gate, gain switched residue amplifier, 8-bit DAC, 4-bit DAC, and n-channel JFET device test patterns. We expect wafer-level performance data including functional yield, amplifier loop gain, bandwidth, offset, and linearity to be available in late August. Analyses of dc linearity and yield of each DAC approach will allow selection of the lowest-risk, highest-performance circuit for the final 12-bit ADC design. In addition, JFET device-matching and W/L ratio-scaling data will be folded into the complete 12-bit ADC design.

Lastly, a $5 \times 5 \mu\text{m}^2$ version of the 400-MHz, $7 \times 7 \mu\text{m}^2$ 5-bit ADC has been included on the April bar. Only minor metal modifications were required to complete the upgrade since the old $7 \times 7 \mu\text{m}^2$ devices were replaced with a metal-1 compatible version of the new $5 \times 5 \mu\text{m}^2$ device. To minimize design time, power scaling of the $5 \times 5 \mu\text{m}^2$ 5-bit ADC was not performed. A maximum clock frequency greater than 1-GHz is expected if the $5 \times 5 \mu\text{m}^2$ target device parameters are attained.

Hughes efforts in May and June continued to focus on the detailed circuit design and layout capture of the complete monolithic 12-bit ADC. During May, a differential interface between the sample-and-hold and DAC was added to the 12-bit ADC architecture. This feature will improve the noise immunity of the design and minimize the impact of process parameter variations, with a minimal impact on the circuit design completed to date.

A significant amount of the circuit design for the 12-bit ADC has been completed this quarter. Circuit design of a low-power version of the 5-bit quantizer and the majority of the circuit design for the S/H, gain-switch amplifier, and DAC have been completed. Schematic capture of 12-bit ADC cells for layout-versus-schematic (LVS) automated verification has begun. A preliminary set of process design rules for the 12-bit ADC will begin in July.

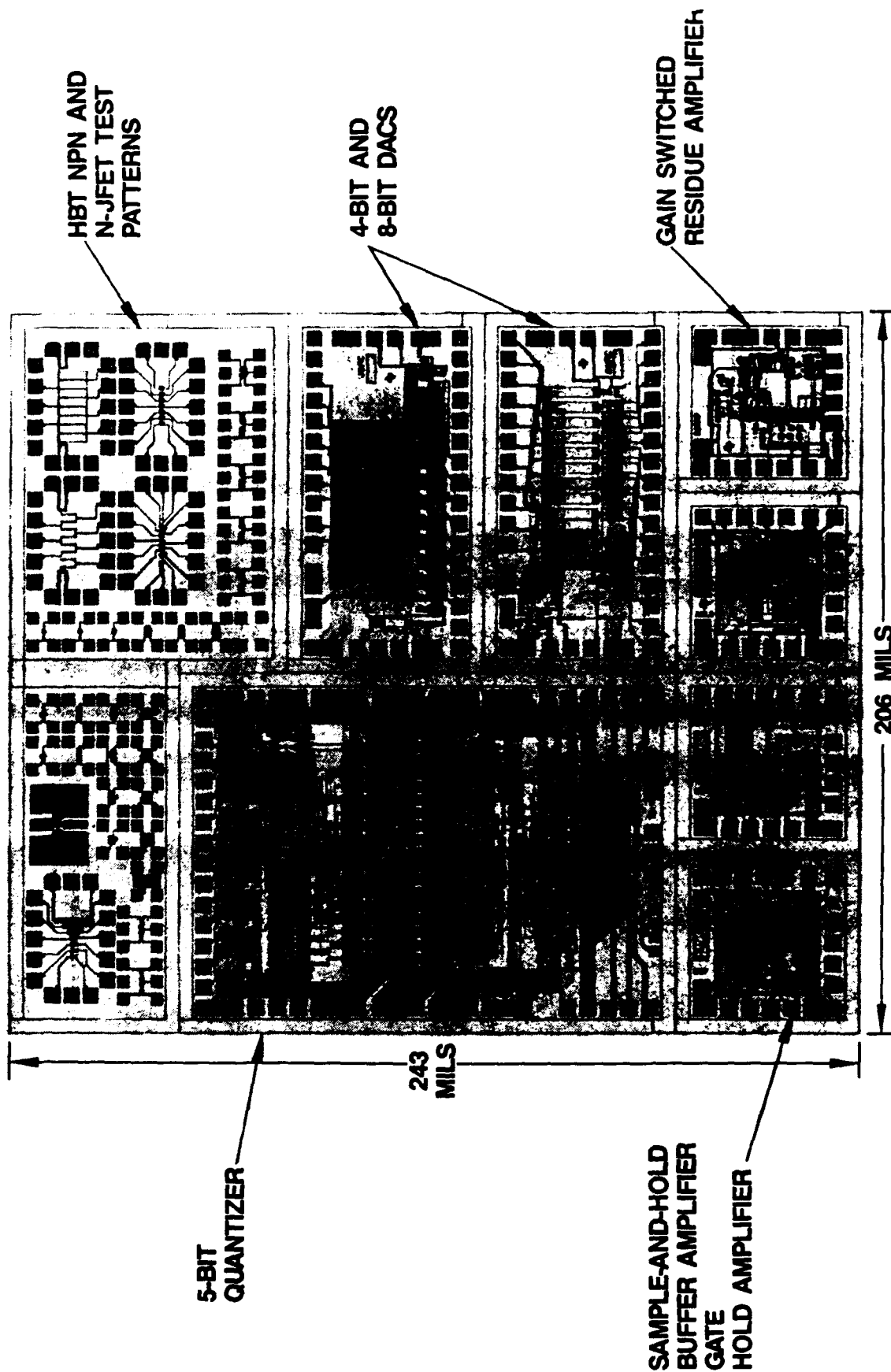


Figure 7. 12-bit 20 MSPS/Watt building block mask set.

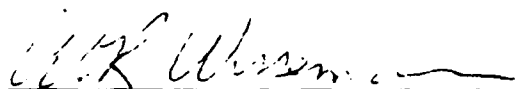
In response to DARPA program office inquiries a cost, complexity, and power impact study of adding a 16:1 analog multiplexer and front-end prescaler to the 12-bit ADC was performed. Given process evolution to $2 \times 5 \mu\text{m}^2$ emitters, the 16:1 mux/prescaler feature could be added to the 12-bit ADC for 400 mW. Total 12-bit ADC system power would be 1.4 W/20 Msps. A rough-order-of-magnitude (ROM) cost and design for the 16:1 mux/prescaler has been completed and a white paper is being prepared for the DARPA program office.

IV. ADC PROCESS TRANSFER TO PILOT LINE

Work began on 1 June to transfer the ADC process from the CRL development laboratory to the DSEG GaAs Pilot Line. ADC masks for the Nikon 5X stepper have been ordered, which include the latest 5-bit ADC design with the $5 \times 5 \mu\text{m}^2$ emitter transistors. A first-pass pilot line ADC process traveler has been generated and is now in the review cycle. Lot starts should begin in July 1989.

V. PLANS FOR NEXT QUARTER

- Complete detailed circuit design and layout of the monolithic 12-bit ADC
- Demonstrate 5-bit ADC with >1 GHz maximum sampling frequency
- Process 3-inch wafer lot on GaAs digital IC pilot line



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